The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ISIK C. KIZILYALLI, JOSEPH RUDOLPH RADOSEVICH and PRADIP KUMAR ROY

Appeal No. 2005-1998
Application No. 09/516,004

ON BRIEF

Before KRATZ, DELMENDO, and FRANKLIN, Administrative Patent Judges.
KRATZ, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 6-11, which are all of the claims pending in this application.

BACKGROUND

Appellants' invention relates to an integrated circuit or semiconductor device including, inter alia, a field effect transistor gate structure formed on a semiconductor surface region, and source and drain regions formed along the surface region of the semiconductor. The gate structure includes a

conductive layer and an amorphous insulating layer having a dielectric constant greater than 5. Also, the source and drain regions are recited as being self-aligned. Claims 6 and 9 are reproduced below.

6. An integrated circuit comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than five, the insulative layer formed between the conductive layer and the surface region;

a self-aligned source region formed along the surface region and having a second conductivity type; and

a self-aligned drain region formed along the surface region and having a second conductivity type, said gate structure, source region and drain region configured to form an operable self-aligned field effect transistor, said source region and said drain region directly self-aligned with the gate structure.

9. A semiconductor device comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than 5, the insulative layer formed between the conductive layer and the surface region; and

a self-aligned source region and a self-aligned drain region, each formed in the surface region, directly self-aligned

with the gate structure and on a different side of the gate structure,

said gate structure, source region and drain region configured to form a self-aligned field effect transistor characterized by a gate leakage current less than 0.1 amp per cm^{-2} during operation.

In addition to alleged admitted prior art, the prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Shinriki et al. (Shinriki)	5,292,673	Mar. 08, 1994
Endo	5,596,214	Jan. 21, 1997
Yu	6,194,748	Feb. 27, 2001 (Filed May 03, 1999)

Claims 6-8 stand rejected under 35 U.S.C. § 112, first paragraph as lacking written descriptive support in the application, as filed. Claims 6 and 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Yu. Claims 6, 7 and 9-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of alleged admitted prior art at page 7, lines 3-9 of appellants' specification and Shinriki. Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of alleged admitted prior art at

page 7, lines 3-9 of appellants' specification, Shinriki and Endo.

We refer to the brief and reply briefs and to the supplemental answer for a complete exposition of the opposing viewpoints expressed by appellants and the examiner concerning the issues before us on this appeal.

DISCUSSION

Upon review of the respective positions advanced by appellants and the examiner with respect to the rejections that are before us for review, we find ourselves in agreement with appellants' viewpoint in that the examiner has failed to carry the burden of establishing a prima facie case of lack of descriptive support. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1471-1472, 223 USPQ 785, 787-788 (Fed. Cir. 1984). Accordingly, we will not sustain the examiner's § 112, first paragraph rejection on this record. However, our disposition of the examiner's anticipation and obviousness rejections is another matter. In this regard, appellants have not persuaded us of any reversible error in the § 102(e) and § 103(a) rejections before us. Thus, we shall affirm the examiner's prior art rejections. Our reasoning follows.

The Rejection for Lack of Descriptive Support

Insofar as the written description requirement is concerned, "the PTO has the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims." In re Wertheim, 541 F.2d 257, 263, 191 USPQ 90, 97 (CCPA 1976). Precisely how close the original description must come to comply with the description requirement of § 112 must be determined on a case-by-case basis. Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 1562, 19 USPQ2d 1111, 1116 (Fed. Cir. 1991). With regard to written descriptive support, all that is required is that appellants' specification reasonably conveys to one of ordinary skill in the art that as of the filing date of the application, appellants were in possession of the presently-claimed invention; how the specification accomplishes this is not material. See In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983); In re Edwards, 568 F.2d 1349, 1351-2, 196 USPQ 465, 467 (CCPA 1978).

The examiner has rejected claims 6-8 as not being described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the

application was filed, had possession of the claimed invention. (answer, page 3).

The examiner has stated that descriptive support in the original disclosure could not be found in the original application disclosure for the claimed requirement that the source/drain regions are self-aligned and configured to form an operable self-aligned field effect transistor. According to the examiner, this is so given subsequent processing steps employed by appellants that would result in ion diffusion under the gate resulting in a final structure that is not self-aligned. See, e.g. pages 3 and 4 of the answer.

Concerning this matter, at page 7, lines 3-7 of the subject specification, appellants provide a detailed description as follows:

> As is common to current semiconductor processing the source/drain regions 21 and 22 are self-aligned with respect to the gate structure 13. That is, after gate formation they are formed by ion implantation of dopant material into portions of the wafer surface 11 overlying the regions 21 and 22, i.e., on opposing sides of the gate structure 13. Other techniques for providing dopants to the regions 21 and 22 may be used as well.

At page 7, lines 18-22 of their specification, appellants further disclose that:

> In the preferred embodiment portions 23 and 24 of the wafer surface 11 overlying the intended source/drain regions 21 and 22 are selectively irradiated to heat certain exposed regions including the source/drain regions 21 and 22. The radiation elevates the temperature of the intended source/drain regions to such temperature as will allow diffusion of the implanted dopant to desired locations.

The examiner further explains at page 8 of the answer that:

> Although [appellants'] figure 2 depict[s] the source and drain regions being formed self-aligned with the gate structure, the device of figure 2 is not operable, since no reflective/protective layer is present over the gate structure and further processing steps are required to render the device operable. The further processing steps required to render the device operable diffuse the source and drain regions under the gate, and thus obtaining a device wherein the source and drain regions are not self-aligned with the gate. The device of figures 1 and 3 clearly does not comprise self-aligned source and drain regions as the subsequent processing steps diffuse the source and drain regions under the gate.

The examiner's supposition of non-alignment is principally based on alleged dopant migration under the gate during additional processing steps in forming an operable transistor.[1]

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[1] While appellants seemingly argue at page 8 of the brief that the additional steps in forming a drain extension region (62, drawing figure 5) represents another embodiment that is not consistent with the claimed operable self-aligned transistor, we disagree with that argument in that Figure 5 is described as illustrating a subsequent phase of the manufacture of an integrated circuit device that was illustrated in Figure 1 at an earlier stage of fabrication. See page 5 of appellants' specification. In this regard, the formation of a drain extension region does not negate the self-aligned formation of

However, that theory does not meet the examiner's burden of proving that self-alignment of an operable field effect transistor is not supported by the record before us. In this regard, we further note that the term "aligned" is consonant with describing device features that are in proper relative position after using gate structure in a self-aligning method as recited in appellants' specification, at page 7 thereof, as referred to above.[2]

Here, the examiner simply has not made the case as to why the so rejected claims would have been construed as describing possession of a new concept or invention not conveyed by the original disclosure for reasons set forth above and in the briefs. Consequently, on the present record, we find ourselves in agreement with appellants' basic position that the original

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the drain region with gate structure.

[2] The term "self-aligned" as used in appellants' claims does not require a strict linear or precisely parallel relationship of edges of the source or drain regions and the gate structure sidewalls but rather would encompass a proper relative positioning of those features within tolerances as would be understood by one of ordinary skill in the art, including overlap caused by lateral diffusion of ions, after using gate structure as a mask. See, e.g., page 318 of Volume 2 of Wolf, Silicon Processing For the VLSI ERA, attached to appellants' brief, and appellants' drawing figures 3 and 5, which depict some overlap of appellants' self-aligned source/drain regions with the gate structure.

disclosure reasonably conveys to the ordinarily skilled artisan that appellants had possession of the claimed subject matter, a position that the examiner has not effectively refuted by the rationale presented for the stated rejection. Therefore, the examiner's rejection under § 112, first paragraph, with regard to the alleged lack of descriptive support cannot be sustained.

§ 102(e) Rejection

Appellants argue claims 6-8 as a group and claims 9-11 as another group. See page 5 of the brief. However, for this rejection, only claims 6 and 7 are involved. Therefore, we select claim 6, as the representative claim.

Appellants do not dispute the examiner's determination that Yu discloses an operable integrated circuit field effect transistor including: (1) a semiconductor material of a first conductivity type having a surface region; (2) a field effect transistor gate structure formed on the surface region, including a conductive layer and an amorphous insulative layer having a dielectric constant above 5; (3) a source region formed on the surface region having a second conductivity type; and (4) a drain region formed on the surface region and having a second conductivity type, as called for in representative claim 6.

Rather, appellants hinge their arguments against the examiner's anticipation rejection of claims 6 and 7, on their assertions that Yu does not disclose that the source and drain regions of Yu's transistor are self-aligned, as required in appealed independent claim 6. In this regard, appellants argue that the claimed self-aligned source region and self-aligned drain region represent distinct structural features not disclosed by Yu.

At page 4 of the reply brief, appellants explain that:

> Appellant's invention is distinguished from Yu because the selective annealing process of the subject invention can be carried out after the amorphous insulative layer is formed and the source and drain regions are formed self-aligned with the gate structure, and without changing the high dielectric constant (k>5) characteristic of the amorphous insulative layer.

That explanation stands in contrast to appellants' assertions (brief, pages 10-13) that the claimed product is not defined, at least in part, by a product-by process limitation in calling for self-aligned source and drain regions. Of course, appellants can not have it both ways.

From our perspective and as evidenced by the selections from Volumes 1 and 2 of Wolf, Silicon Processing For the VLSI ERA (copies attached to the brief), the claim term, "self-aligned,"

as applied to forming source and drain regions refers to employing gate structure as a mask during ion doping as a step in forming the source and drain regions, which results in the so called self-aligned source and drain regions. Those regions are aligned with the gate at least to the extent some gate structure is used as a mask as part of their formation. Moreover, that so called self-alignment does not preclude diffusion of implanted ions under the gate resulting in overlap of the gate structure with the source and drain regions. While no particular method of using the gate as a mask is required by those claim terms, it is clear that those claim terms do invoke a broad product-by-process limitation. This is consistent with appellants' description at page 7, lines 3-7 of their specification (reproduced infra). In this regard, we give those claim terms their broadest reasonable interpretation as they would be understood by one of ordinary skill in the art when read in light of appellants' specification. See In re Sneed, 710 F.2d 1544, 1548, 218 USPQ 385, 388 (Fed. Cir. 1983). In this regard, we determine that the claimed product requires source and drain regions that would correspond to the source and drain regions that are obtained by employing a gate structure or equivalent as a mask during ion doping by any known method of so doing. Of course, such a claim construction

also includes equivalent source and drain region arrangement obtained by another method within the scope thereof because the claims are not limited to a self alignment process but rather the product produced thereby. Consequently, we agree with the examiner's anticipation position as set forth in the supplemental answer, based on the broadest reasonable construction of those disputed claim terms, as discussed above.

While Yu does teach that an amorphous titanium dioxide gate layer (34) and gate conductor layer (36) can optionally be deposited after dopant activation, as argued by appellants, Yu nonetheless describes using gate (18) as a mask for ion implantation in forming the drain and source regions and extension via a two step ion doping method. See, e.g., column 5, lines 30-45 of Yu. Thus, Yu does disclose self-aligned source and drain regions, as broadly claimed.[3] Moreover, Yu clearly

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[3] We note that self-aligned source and drain regions, as here claimed are not limited to a product made by a particular method of using a gate structure as a mask in the formation of those regions, as appellants have suggested at page 10 of the brief. As such, arguments about further processing of a gate structure by adding layers thereto after using the gate structure as a mask are entitled to little weight. Moreover, the claimed source/drain regions are not defined as being of a particular depth or ion loading density so as to exclude lightly doped source and/or drain extension regions. Nor do the claims require a particular degree of alignment beyond any attainable by any self-alignment process. When the claim does not recite allegedly

discloses that amorphous layer 34 is protected from high heat either by depositing that layer after all high heating processes are completed or by using lower temperature processes after the layer 34 is deposited. See, e.g., column 5, lines 5-9 of Yu. As another option, Yu suggests employing a damascene process in forming a self aligned structure. See, e.g., column 5, lines 9-12 and column 1, lines 6-28 of Yu.

Given the above, we are not persuaded by appellants' arguments and the evidence referred to in the brief. In this regard, the references to the numerous patents cited at pages 11-13 of the brief concerning prior art self-aligned structures strengthens rather than diminishes the examiner's anticipation position in that those referred to patents, as reported by appellants, make clear that self-aligned source and drain features, as broadly claimed here, are commonly arrived at through a variety of gate structure, drain region and source region formation techniques. In this regard, appellants have not established that any of those referred to patents teaches that the source and drain regions of Yu, the patent reference that is

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distinguishable features, "appellant[s] cannot rely on them to establish patentability." In re Self, 671 F.2d 1344, 1350-1351, 213 USPQ 1, 7 (CCPA 1982).

actually applied and at issue here, are not self-aligned given the disclosure of Yu concerning using gate structure as a mask.[4] Moreover, we note that a patentee can be his/her own lexicographer. Thus, appellants reliance on patents issued from other applications in arguing for a narrow claim interpretation for terms employed in claims of the instant application is misplaced.

It follows that, on this record, we will sustain the examiner's anticipation rejection of claims 6 and 7 for reasons set forth in the answer and above.

§ 103(a) Rejections

Claims 6, 7 and 9-11

For reasons as discussed above with regard to the anticipation rejection of claims 6 and 7 over Yu, we find that the circuit of claims 6 and 7 are also prima facie obvious over the applied references. This is so because anticipation is the epitome of obviousness. A disclosure that anticipates under

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[4] Indeed, U.S. Patent No. 5,780,892 to Chen, that is referred to by appellants at page 12 of the brief in rebuttal, suggests that the source and drain regions can be self-aligned even when gate layers are formed after source and drain formation. See, e.g. column 5, lines 1-12 of Chen. See In re Hedges, 783 F.2d 1038, 1039-40, 228 USPQ 685, 686 (Fed. Cir. 1986).

35 U.S.C. § 102 also renders the claim unpatentable under 35 U.S.C. § 103, for "anticipation is the epitome of obviousness." Jones v. Hardy, 727 F.2d 1524, 1529, 220 USPQ 1021, 1025 (Fed. Cir. 1984). See also In re Fracalossi, 681 F.2d 792, 794, 215 USPQ 569, 571 (CCPA 1982).

Yu is concerned with maintaining the amorphous layer of the gate in that amorphous state as evidenced by Yu's teachings concerning that high dielectric material and the advantages associated therewith, as well as the manner in which the device is formed so as to avoid high temperature treatment of that material. Moreover, even if we agreed with appellants that Yu did not form self-aligned source and drain regions, which we do not so believe, it would have been obvious to one of ordinary skill in the art to form the source/drain regions of Yu in such a self-aligned format given the additional teachings of the admitted prior art concerning the conventionality of the self-alignment formation of source/drain regions. See page 7, lines 3-9 of their specification and the examiner's uncontested finding that such represents an admission of prior art by appellants.

Appellants (reply brief filed January 21, 2005, page 7) assert that "the conventional art precluded the use of this feature [self-aligned source/drain regions] in combination with

the feature of an amorphous insulative layer hav[ing] the dielectric constant greater than 5." However, appellants have not substantiated that assertion with persuasive evidence for reasons discussed above with respect to the anticipation rejection. Thus that reply brief argument, as well as the conforming arguments set forth at pages 13-16 of the brief, are not found convincing of any reversible error in the examiner's obviousness assessment.[5] Consequently, we agree with the examiner's obviousness determination as to claims 7 and 8 for reasons set forth in the answer and above.

As for appealed claims 9-11, we select claim 9 as the representative claim. Here, appellants additionally argue that the claim 9 requirement for a gate leakage current less than 0.1 amp per square centimeter during operation further differentiates claims 9-11 over Yu. We disagree because Yu discloses a semiconductor device that includes each of the features set forth in representative claim 9 but for the recited gate leakage current property for reasons stated above with respect to the

[5] Because we find that the teachings of Yu alone or in combination with the admitted prior art are sufficient to establish the obviousness of the claimed subject matter, we need not further discuss the further teachings of Shinriki, as also relied upon by the examiner in the answer.

anticipation rejection of claims 6 and 7. In this regard, the only argued distinction other than that intrinsic leakage property is the requirement for self-aligned source/drain regions. However, that requirement is fairly met, prima facie, by Yu given the demonstrated breadth of those self-aligned features for reasons set forth above. As for the recited gate leakage current, it would have been reasonable to expect that Yu's semiconductor device field effect transistor gate structure would possess such a characteristic given the commonality of the transistor structure of Yu and that required by representative claim 9. In this regard, we note that appellants attribute such lower leakage currents with retaining tantalum pentoxide in an amorphous state, a state that Yu expressly teaches should be maintained for low leakage current by avoiding high temperature treatment thereof. See column 2, lines 15-18 and column 5, lines 5-12 and 50-55 of Yu. On this record, appellants have not demonstrated that one of ordinary skill in the art following the teachings of Yu would not have reasonably arrived at a semiconductor device transistor structure having the claimed leakage characteristics. See In re Fitzgerald, 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980); In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

Consequently, we agree with the examiner that claims 9-11 would have been obvious, prima facie, to one of ordinary skill in the art given the applied prior art teachings, based on this record. Appellants have not persuasively refuted that evidence of obviousness, on this record, for reasons discussed above. Accordingly, we shall affirm the examiner's obviousness rejection of claims 67 and 9-11.

Claim 8

As for the examiner's separate obviousness rejection of dependent claim 8 further applying Endo thereto, appellants do not base their arguments on the added silicon oxide layer thereof. Rather, appellants maintain that claim 8 is non-obvious based on the features of independent claim 6. However, for reasons discussed above, we do not find that argument persuasive. It follows that we shall also sustain the examiner's separate obviousness rejection of claim 8, on this record.

CONCLUSION

The decision of the examiner to reject claims 6-8 under 35 U.S.C. § 112, first paragraph as lacking written descriptive support in the application, as filed, is reversed. The decision of the examiner to reject claims 6 and 7 under 35 U.S.C. § 102(e) as being anticipated by Yu; to reject claims 6, 7 and 9-11 under

35 U.S.C. § 103(a) as being unpatentable over Yu in view of alleged admitted prior art at page 7, lines 3-9 of appellants' specification and Shinriki; to reject claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of alleged admitted prior art at page 7, lines 3-9 of appellants' specification, Shinriki and Endo is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

PETER F. KRATZ
Administrative Patent Judge

ROMULO H. DELMENDO
Administrative Patent Judge

BEVERLY A. FRANKLIN
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

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